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--26. A semiconductor device as in claim 25 wherein the pad metal covers said active element.

27. A semiconductor device as in claim 16, further comprising another barrier metal layer, said another barrier metal layer is provided on the passivation film and the pad metal which is exposed by a window in the passivation film.--

REMARKS

Reconsideration of this application is respectfully requested.

The rejection of claims 22 and 25 as being indefinite has been overcome by amendment. The references to a "metal wire" have been clarified in the claims.

The rejection of claims 14, 15, 22 and 25 as being anticipated by Ng (US Patent No. 5,843,839) are traversed.

There is no anticipation because Ng does not disclose a pad metal that covers an active element, nor an interlayer insulating film and barrier metal layer between a pad metal layer and an active element.

The claims have been amended to make clear that the active elements have diffusion layers and a gate. Support for defining active elements as having at least two diffusion layers and a gate is in the specification at page 16, lines 9 to 15, and is shown in Figures 5, 7, and 14 to 18. Moreover, the independent claims (except for independent claim 25) have been amended to make clear that the pad metal layer covers the active element, as is disclosed in the specification at, for example, page 34, line 10 to page 35, line 3, and shown in Figures 5, 7, 14 and 18. Furthermore, claim 16 has been amended to

recite the aperture in the passivation film shown in Figure 9, and described in the specification at page 36, lines 15 to 19, and see also page 20, lines 7 to 12.

Ng, as shown in its Figure 12, has a metal contact column for a semiconductor device that connects an active source/drain region (7) on a substrate (1) to a top (fourth) interconnect metallization structure (24). The metal contact column extends between the source/drain region and the fourth interconnect metallization structure. The Ng contact column includes a contact plug (10(b)), a first level interconnect metallization structure (12b), barrier layer (40), second level interconnect metallization structure (17b), plug (20), third level interconnect metallization structure (22), and barrier layer (41). A second contact column, opposite the first column, is formed by 10(c), 12(c), 40, 17(c), 20, 22 and 41. A pair of contact columns are formed on opposite sides of dielectric layers (14, 16, 18) and insulator layer 23.

Unlike the present invention, the contact columns disclosed in Ng do not cover the active element, interlayer insulating film(s) or any barrier metal layer. The Ng interlayer contact columns stand on either side of the dielectric layers and insulating layer. The substrate area covered by the Ng horizontal arrangement of contact plug – dielectric/insulating layers – contact plug is seemingly greater than the area covered by the present invention where the contact plug covers the barrier metal layer interlayer insulating films, and active element.

Between the plug columns of in Ng are three stacked levels. The lower level is formed of dielectric layers (14, 16) and SOG level 15. The middle dielectric level (18)

and upper insulating level (23) also appear to be each formed of three layers. Unlike the present invention, Ng does not disclose a structure in which a pad metal is provided on an interlayer insulating film via a barrier metal layer at an upper portion of an active element which includes at least two diffusion layers and a gate electrode. In Ng, the pad metal does not substantially cover the two diffusion layers and the gate electrode of the active element. Moreover, the pad metal is not provided on the interlayer insulating film via the barrier metal layer, as in the present invention.

Further, Ng does not disclose multiple interlayer insulating films between wire layers as recited in claim 25. In Ng (as shown in FIG. 12) the barrier layers (40, 41) are provided (i) between the first level interconnect metallization structures (12b, 12c) and the second wiring metal structures (17b, 17c), and (ii) between the third level interconnect metallization structure (22) and the fourth interconnect metallization structure (24). The dielectric layer (18) is provided between the second level interconnect metallization structures (17b, 17c) and the third level interconnect metallization structure (22). Therefore, Ng does teach interlayer insulating films provided between metal wiring layers, as called for in claim 25.

Moreover, unlike the present invention, Ng does not suggest a technique to prevent exfoliation of lower portions of an electrode pad which is brought about by a local damage given upon bonding the electrode pad. Prevention of exfoliation is an advantage of the present invention. Spec. pp. 11-13. A barrier metal made of a refractory metal such as titantungsten and the interlayer insulating film made of PSG or BPSG do not

adhere to each other; and an interlayer insulating film made of a mechanically fragile spin-on-glass (SOG) layer exists under the electrode pad. Because Ng does not disclose a metal pad over a barrier level or interlayer insulating film, it does not address the exfoliation problem solved by the present invention.

The rejection of dependent claim 16 as being obvious over Ng in view of Goto (US Patent No. 5,306,936) is traversed for at least the same reasons stated above with respect to claim 15, on which depends claim 16.

Goto (see Figs. 1g, 2, 6, and 7) discloses a passivation film (16, 30, 50) formed of a silicon nitride which covers a silicon oxide film (14, 28b, 48b) and a metal wiring (15, 29, 49). See e.g., Goto column 2, lines 48 to 58, column 6, lines 54 to 65, column 8, lines 1 to 4. However, Goto discloses a structure in which the silicon nitride used as the passivation film is provided on a whole surface of a substrate (column 2, lines 55 to 58, column 6, lines 61 to 65). Goto does not disclose a relation between the pad metal and an opening portion (window-opening portion) of the passivation film. Further, Goto does not suggest that stress induced by bonding can be alleviated by a passivation film that covers a large part of the pad metal. It would not have been obvious to apply Goto to modify the semiconductor device disclosed in Ng in order to form the claimed invention.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made**."

All claims are in good condition for allowance. If any small matter remains outstanding, the Examiner is requested to telephone applicants' attorney. Prompt reconsideration and allowance of this application would be appreciated.

Respectfully submitted,

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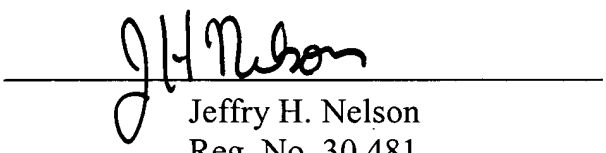
By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Amend claims 14, 15, 16, 22 and 25 as follows:

14. (Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a metal [wire] wiring layer provided on said active element;

an interlayer insulating film [formed so as to cover] covering said active element;

a pad metal for an electrode pad, said pad metal being provided on said interlayer insulating film; and

a barrier metal layer provided on said active element with said interlayer insulating film therebetween, so that said pad metal is provided on said barrier metal layer and covering said active element, wherein:

said interlayer insulating film has at least a level difference compensating film for compensating a level difference of the metal [wire] wiring layer; and

a portion of said level difference compensating film under said pad metal is removed.

15. (Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a metal [wire] wiring layer provided on said active element;

an interlayer insulating film [formed so as to cover] covering said active element;

a pad metal for an electrode pad, said pad metal being provided on said interlayer insulating film; and

a barrier metal layer provided on said active element with said interlayer insulating film therebetween, so that said pad metal is provided on said barrier metal layer and covering said active element,

wherein:

said interlayer insulating film has at least a level difference compensating film for compensating a level difference of the metal [wire] wiring layer; and

said level difference compensating film is formed to a minimum thickness necessary for compensating the level difference of the metal [wire] wiring layer.

16. (Amended) A semiconductor device as set forth in claim 14, further comprising a passivation film, said passivation film being formed so as to cover a large part of said pad metal, and an aperture in said passivation film having an edge adjacent an inside edge of said pad metal.

22. (Twice Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a lower interlayer insulating film formed so as to cover said active element;

a metal [wire] wiring layer provided on said lower interlayer insulating film;

an upper interlayer insulating film formed so as to cover said metal [wire] wiring layer; and

a pad metal for an electrode pad, said pad metal being provided on said upper interlayer insulating film and covering said active element,

another metal wiring layer formed on the active element;

wherein each of said lower and upper interlayer insulating films have a trilaminar structure, each of a first layer and a third layer[s] of the trilaminar film being a silicon nitride film or a silicon oxide film, while a second layer of the trilaminar film being formed of spin-on-glass;

[the semiconductor device further comprising a metal wire formed on the active element, the film formed of spin-on-glass in the interlayer insulating film being] and the second layer of the upper interlayer insulating film formed to a minimum thickness necessary for compensating the level difference of the metal [wire] wiring layer.

25. (Twice Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a first metal wiring layer formed on the active element;

a plurality of other metal [wires] wiring layers above said active element; and

a plurality of interlayer insulating films each being provided between a pair of said plurality of other metal [wires] wiring layers,

wherein each interlayer insulating film has a multilayer structure including at least [a structure in which] a [film formed by the] spin-on-glass film [is] sandwiched [by] between insulating films [each of which is either] formed of a silicon nitride film or a silicon oxide film;

[the semiconductor device further comprising a metal wire formed on the active element,] further wherein the film formed of spin-on-glass in the interlayer insulating film being formed to a minimum thickness necessary for compensating [the] a level difference of [the metal wire] one of said plurality of other metal wiring layers;

a pad metal for an electrode pad, said pad metal being provided on said interlayer insulating film.